EENG 5550 HW 1 Report Template

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# Block diagram OF MULTIPLEXER 32 TO 1

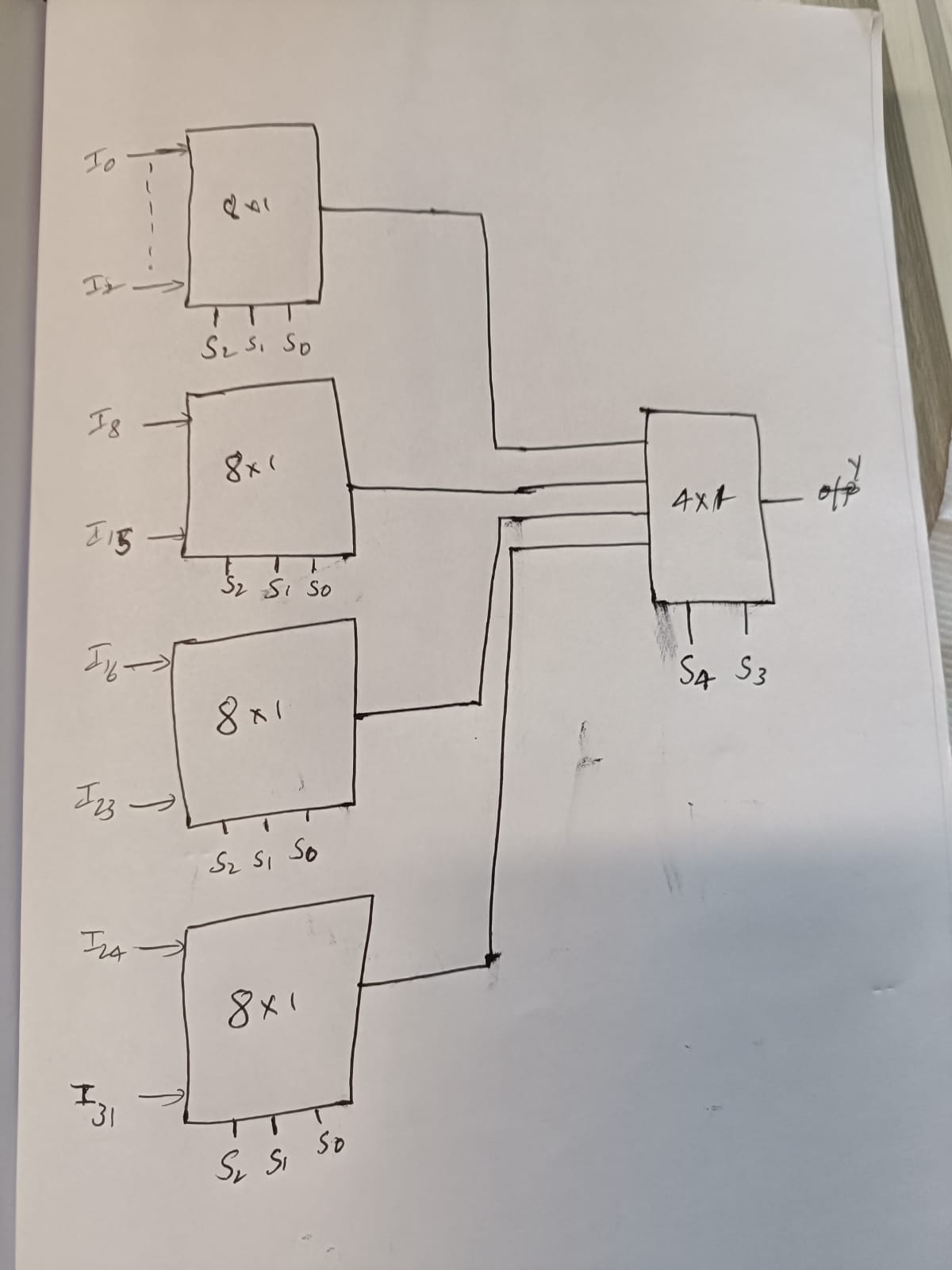


Figure 32 to 1 multiplexer

* Overall Component: 32 to 1 multiplexer
* Overall ports:
  + Inputs:
    - I0, I1, I2, I3, I4, I5, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15, I16, I17, I18, I19, I20, I21, I22, I23, I24, I25, I26, I27, I28, I29, I30, I31
    - Sel
  + Outputs:
    - Y
* Subcomponents:
  + Multiplexer 8 to 1
  + Multiplexer 4 to 1
* Necessary intermediate signals:
  + S0
  + S1
  + S2
  + S3

## Design\Algorithm ex:

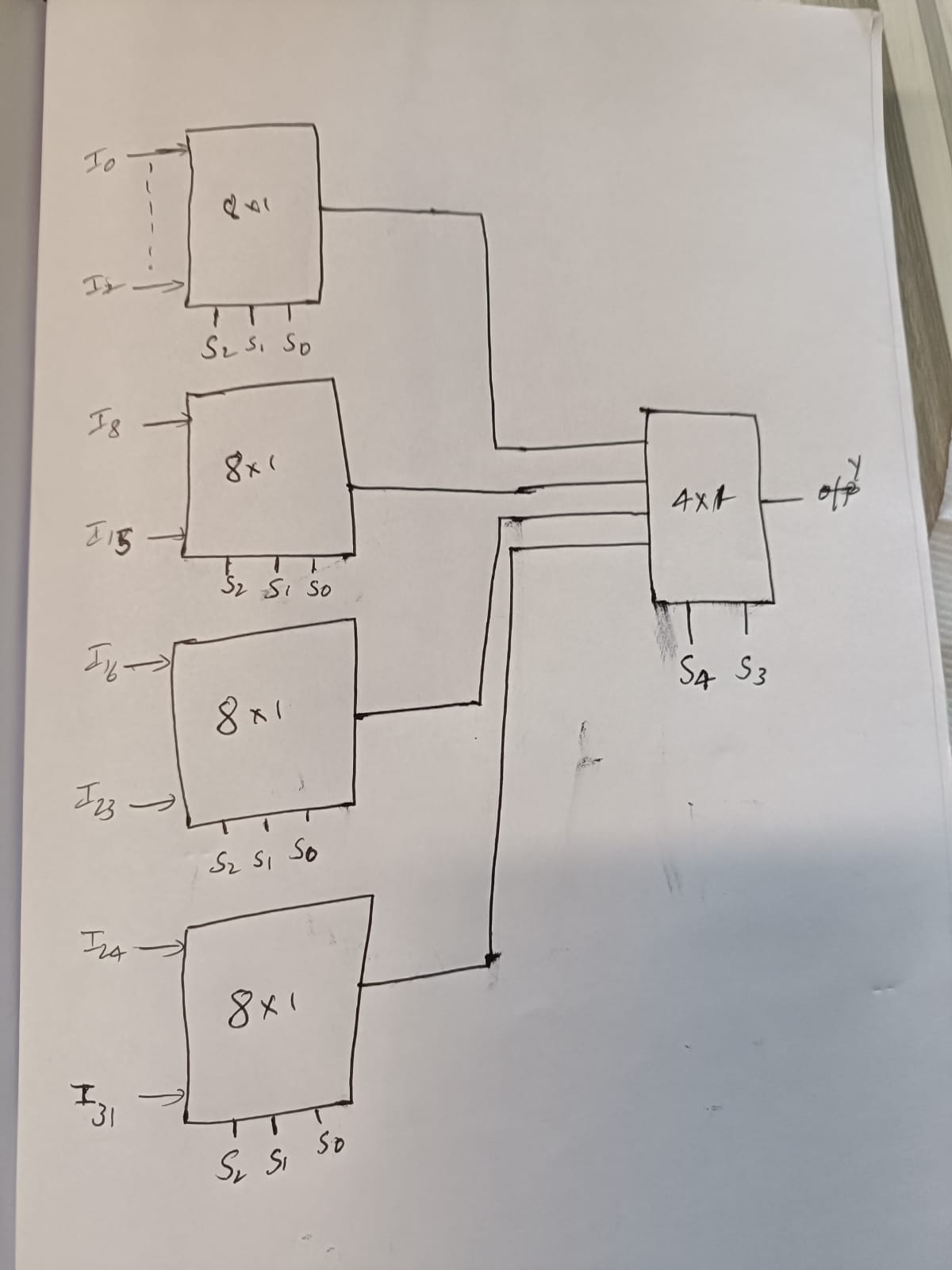


Figure 3 – 32 to 1 multiplexer

* Overall Component: 32:1 multiplexer (mux)
* Overall ports:
  + Inputs:
    - I0: 5 bits -> 00011
    - I1: 5 bits -> 00100
    - I2: 5 bits -> 11010
    - I3: 5 bits -> 00101
    - I4: 5 bits -> 00110
    - I5: 5 bits -> 00111
    - I6: 5 bits -> 01000
    - I7: 5 bits -> 01001
    - I8: 5 bits -> 01010
    - I9: 5 bits -> 01011
    - I10: 5 bits -> 01100
    - I11: 5 bits -> 01101
    - I12: 5 bits -> 01110
    - I13: 5 bits -> 01111
    - I14: 5 bits -> 10000
    - I15: 5 bits -> 10001
    - I16: 5 bits -> 10010
    - I17: 5 bits -> 10011
    - I18: 5 bits -> 10100
    - I19: 5 bits -> 10101
    - I20: 5 bits -> 10110
    - I21: 5 bits -> 10111
    - I22: 5 bits -> 11000
    - I23: 5 bits -> 11001
    - I24: 5 bits -> 11010
    - I25: 5 bits -> 11011
    - I26: 5 bits -> 11100
    - I27: 5 bits -> 11101
    - I28: 5 bits -> 11110
    - I29: 5 bits -> 11111
    - I30: 5 bits -> 00001
    - I31: 5 bits -> 00011
    - Sel: 5 bits -> select line input
      * Sel4: MSB (bit 4)
      * Sel3: (bit 3)
      * Sel2: (bit 2)
      * Sel1: (bit1)
      * Sel0: LSB(bit 0)
  + Outputs:
    - :Y single bit -> output

**Representation of design:**

|  |  |
| --- | --- |
| Select input | Resulting output |
| 00000 | I0 |
| 00001 | I1 |
| 00010 | I2 |
| 00011 | I3 |
| 00100 | I4 |
| 00101 | I5 |
| 00110 | I6 |
| 00111 | I7 |
| 01000 | I8 |
| 01001 | I9 |
| 01010 | I10 |
| 01011 | I11 |
| 01100 | I12 |
| 01101 | I13 |
| 01110 | I14 |
| 01111 | I15 |
| 10000 | I16 |
| 10001 | I17 |
| 10010 | I18 |
| 10011 | I19 |
| 10100 | I20 |
| 10101 | I21 |
| 10110 | I22 |
| 10111 | I23 |
| 11000 | I24 |
| 11001 | I25 |
| 11010 | I26 |
| 11011 | I27 |
| 11100 | I28 |
| 11101 | I29 |
| 11110 | I30 |
| 11111 | I31 |

# Generated RTL Block Diagram\Schematic

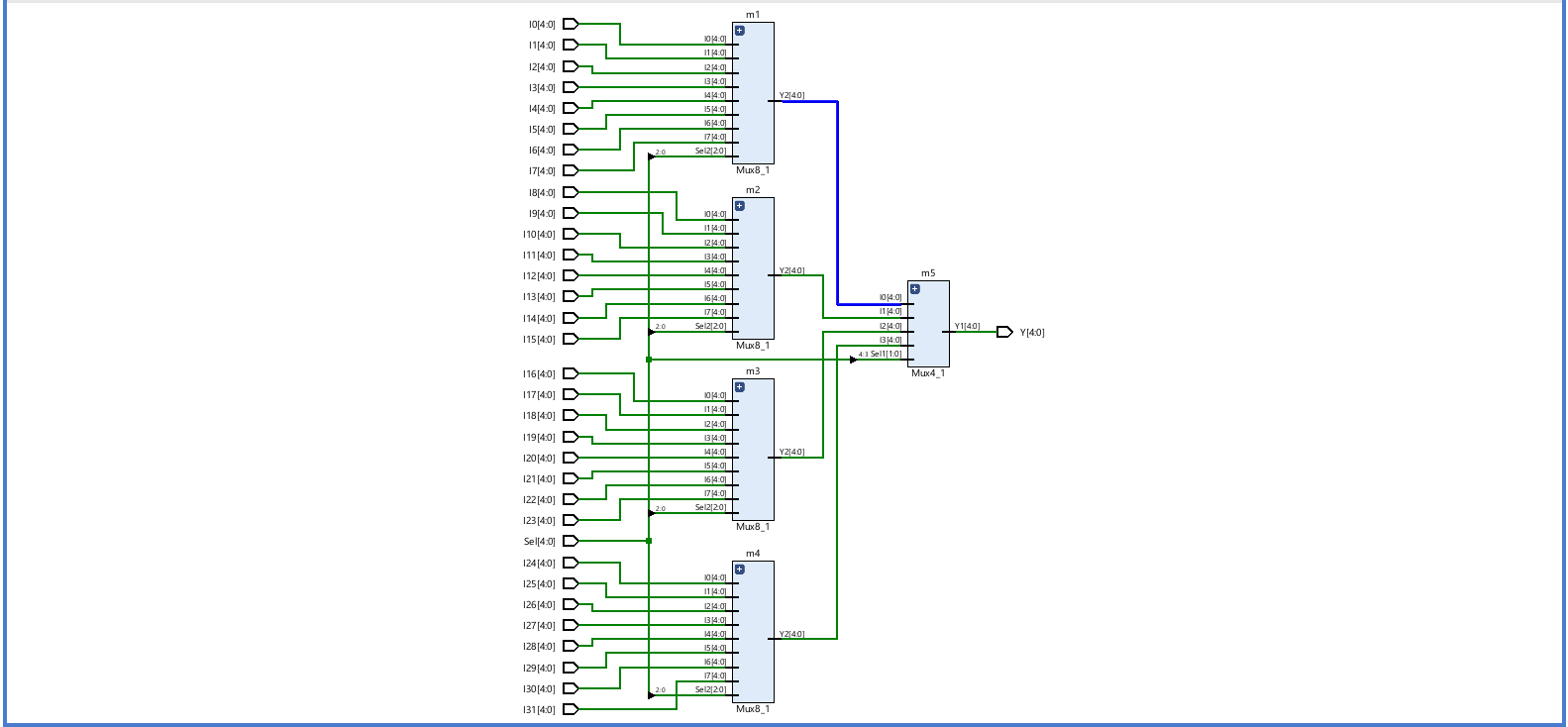
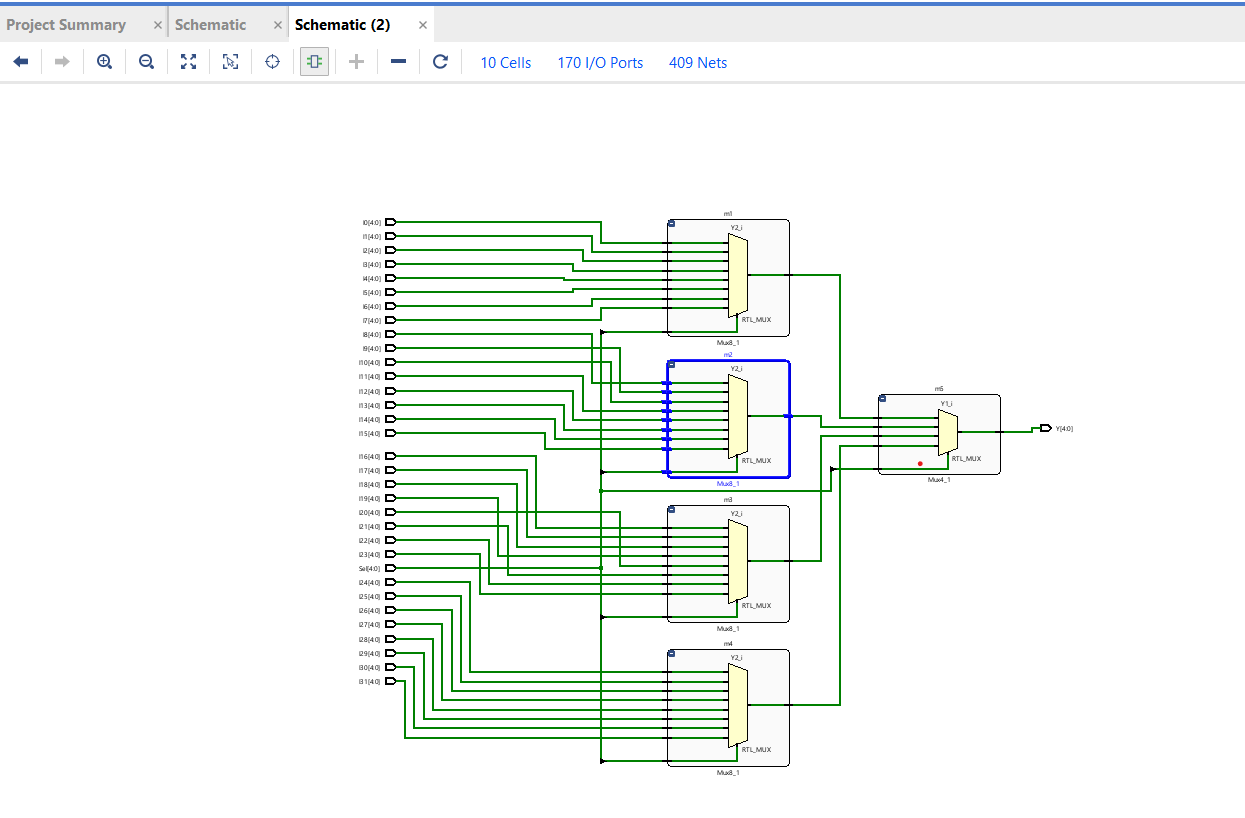


Figure 5 - generated RTL schematic.



# Results

## Waveforms

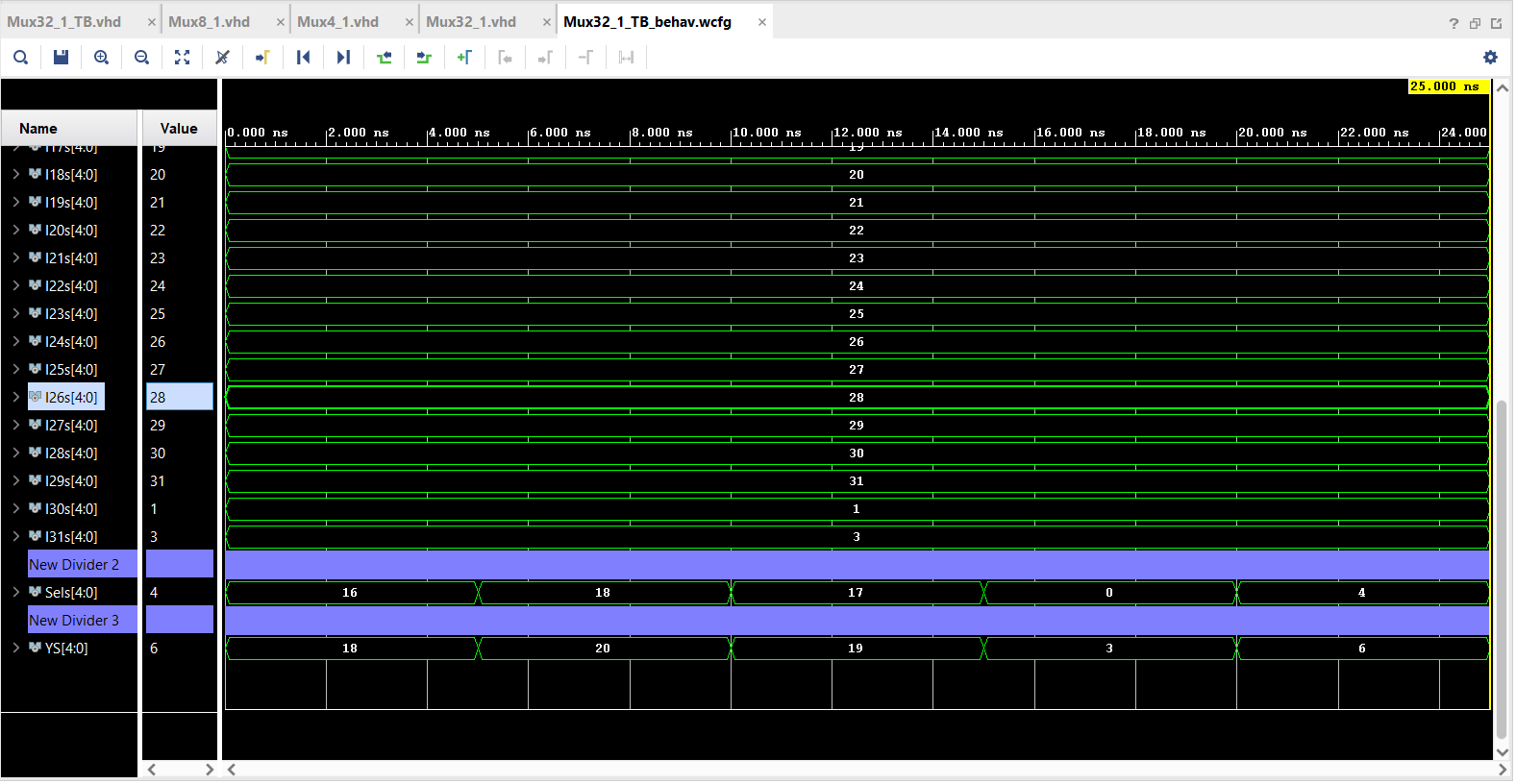


Figure 6 - Waveforms

## Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | calculations | waveforms |  |
|  | Sel | Y | Y | |
| Test case 1: | 10000 | 10010 | 10010 | |
| Test case 2: | 10010 | 10010 | 10010 | |